IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: DENNIS *et al.*	Confirmation No.: 7033
Application No.: 09/715,772	Art Unit: 2111
Filed: November 17, 2000	Examiner: Justin King
For: **Multi-Thread Peripheral Processing Using Dedicated Peripheral Bus**	Atty. Docket: 2222.4210001

Brief on Appeal Under 37 C.F.R. § 41.37

Mail Stop Appeal Brief - Patents

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

A Notice of Appeal from the final rejection of claims 1 - 41 was filed on October 19, 2005. Appellants hereby file one copy of this Appeal Brief, together with the required fee set forth in 37 C.F.R. § 41.20(b)(2).

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

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I. Real Party In Interest (37 C.F.R. § 41.37(c)(1)(i))

The real party in interest in this appeal is the United States Government, as represented by the Secretary of the Navy. In addition, Nanocomm Systems, LLC, located at 2215-B Renaissance Drive, Suite 5, Las Vegas, NV 89119, is a licensee under this application.

II. Related Appeals and Interferences (37 C.F.R. § 41.37(c)(1)(ii))

To the best of the knowledge of Appellants, Appellants' legal representative, and Appellants' assignee, there are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on a decision by the Board of Patent Appeals and Interferences ("the Board") in the pending appeal.

III. Status of Claims (37 C.F.R. § 41.37(c)(1)(iii))

This application was originally filed as U.S. Non-Provisional Application No. 09/715,722 on November 17, 2000 with 41 claims. This application is a continuation of U.S. Provisional Application No. 60/166,686 filed on November 19, 1999. In response to an Office Action mailed June 23, 2003, Appellants filed an Amendment and Reply on October 23, 2003 in which claims 1, 4, 12-14, 17, 24-27, 30, and 38-41 were amended. In response to a Final Office Action mailed December 29, 2003, Appellants filed an Amendment and Reply on February 6, 2004, in which claims 40 and 41 were amended. The Examiner issued an Office Action on December 29, 2004. Applicants filed an Amendment and Reply on April 29, 2005, in which claims 1, 14, 27, 40, and 41 were amended. The Examiner issued a Final Office Action on July 19, 2005, to which Appellants filed a Reply on August 10, 2005, in which no amendments were made.

Claims 1-41 are pending. Claims 1-41 are rejected and are being appealed. A copy of the claims on appeal can be found in the attached Appendix as required under 37 C.F.R. § 41.37(c)(1)(viii).

IV. Status of Amendments (37 C.F.R. § 41.37(c)(1)(iv))

No amendments have been filed subsequent to the Final Office Action dated July 19, 2005. All amendments presented in the Amendment and Reply dated October 23, 2003, the Amendment and Reply dated February 6, 2004, and the Amendment and Reply dated April 29, 2005 have been entered.

V. Summary of Claimed Subject Matter (37 C.F.R. § 41.37(c)(1)(v))

A concise explanation of the invention is provided below for each of the independent claims involved in the appeal. The explanation refers to the specification by page and line number, and to the drawings, if any, by reference characters.

For each independent claim involved in the appeal and for each dependent claim argued separately under the provisions of paragraph (c)(1)(vii), every means plus function and step plus function as permitted by 35 U.S.C. § 112, sixth paragraph, are identified. The structure, material, or acts described in the specification as corresponding to each claimed function are set forth with reference to the specification by page and line number, and to the drawings, if any, by reference characters.

FIG. 1 of the Specification illustrates a multi-processor core 110 interfacing with peripheral units 130 in accordance with the subject matter claimed. Independent claim 1 is directed to an apparatus 100 comprising a peripheral bus 260 (*see* FIG. 2) coupled to a peripheral unit 130 to transfer peripheral information including a command message (*see* FIG. 5A; FIG. 5B) specifying a peripheral operation. (Specification, p. 9, ll. 5-12). Claim 1 is further directed to a processing slice 310 (*see* FIG. 3) coupled to the peripheral bus 260 to execute a plurality of threads including instructions, where one of the threads sends a command message to the peripheral unit. (Specification, p. 9, ll. 13-28). The processing slice 310 comprises a functional unit 450 (*see* FIG. 4) to perform a register operation specified in the instructions dispatched from each of the plurality of threads. (Specification, p. 12, ll. 5-12). The processing slice further executes the instructions from more than one of the plurality of threads concurrently in a clock cycle. (Specification, p. 8, ll. 23-25).

Independent claim 14 and its dependent claims find similar support to the above within the specification. Independent claim 27 and its dependent claims also find similar support to the above within the specification.

Independent claim 40 finds similar support to the above support for claim 1 in the specification, and further claims a plurality of multi-thread processors (*see* FIG. 2, generally) as well as a plurality of peripheral units 130.

Independent claim 41 finds similar support to the above support for claim 1 in the specification, and further claims a multi-thread processor having program base registers 473 and data base registers 462. (Specification, p. 10, ll. 26-29; p. 12, ll. 27-29).

Dependent claim 8 claims the apparatus of claim 1 wherein the processing slice disables the first thread after sending the command message if the command is a wait instruction, whereas in claim 9, the thread continues to execute after sending the command message if the command is a non-wait instruction. (Specification, p. 9, ll. 21-28). Dependent claims 21 and 22 find similar support to the above support for claims 8 and 9 in the specification. Dependent claims 34 and 35 find similar support in the specification.

VI. Grounds of Rejection to be Reviewed on Appeal (37 C.F.R. § 41.37(c)(1)(vi))

The Examiner finally rejected claims 1-12, 14-25, 27-38, and 41 under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent No. 5,815,727 to Motomura ("Motomura").

The Examiner finally rejected claims 13, 26, and 39 under 35 U.S.C. § 103(a) as allegedly being obvious over Motomura in view of U.S. Patent No. 5,418,917 to Hiraoka et al. ("Hiraoka").

The Examiner finally rejected claim 40 under 35 U.S.C. § 103(a) as allegedly being obvious over Motomura in view of U.S. Patent No. 5,938,765 to Dove et al. ("Dove").

Accordingly, the grounds of rejection to be reviewed on appeal are:

A. Ground 1

Whether claims 1-12, 14-25, 27-38, and 41 would have been anticipated by U.S. Patent No. 5,815,727 to Motomura under 35 U.S.C. § 102(b).

B. Ground 2

Whether claims 13, 26, and 39 would have been obvious over U.S. Patent No. 5,815,727 to Motomura in view of U.S. Patent No. 5,418,917 to Hiraoka et al. under 35 U.S.C. § 103(a).

C. Ground 3

Whether claim 40 would have been obvious over U.S. Patent No. 5,815,727 to Motomura in view of U.S. Patent No. 5,938,765 to Dove et al. under 35 U.S.C. § 103(a).

VII. Argument (37 C.F.R. § 41.37(c)(1)(vii))

There are three separate grounds of rejection to be reviewed on appeal.

A. Rejection of claims 1-12, 14-25, 27-38, and 41 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,815,727 to Motomura

A Final Office Action was mailed on July 19, 2005, rejecting claims 1-12, 14-25, 27-38, and 41 under 35 U.S.C. § 102(b) as allegedly being anticipated by Motomura. Appellants' remarks focus mainly on independent claims 1, 14, 27, and 41, because any claim which depends from a patentable independent claim is also patentable at least by virtue of its dependency. Additional and separate remarks will cover dependent claims 8, 9, 22, 23, 34, and 35 specifically.

In proceedings before the Patent and Trademark Office, the examiner bears the burden of establishing a *prima facie* case of anticipation based on prior art which must disclose each limitation of the claims. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). Because the Motomura reference fails to disclose each limitation of the claims, the rejection of claims 1-12, 14-25, 27-38, and 41 must be reversed.

1. The Anticipation Rejection with Respect to Claims 1-7 and 10-12 is in Error and Must be Reversed

Motomura does not teach or suggest each feature of Appellants' independent claim 1. Independent claim 1 recites "an apparatus", wherein the apparatus includes:

> a peripheral bus coupled to a peripheral unit to transfer peripheral information including a command message specifying a peripheral operation; and
>
> a processing slice coupled to the peripheral bus to execute a plurality of threads comprising instructions, the plurality of threads including a first thread sending the command message to the peripheral unit;

> wherein the processing slice comprises a functional unit to perform a register operation specified in the instructions dispatched from each of the plurality of threads; and
>
> wherein the processing slice executes the instructions from more than one of the plurality of threads concurrently in a clock cycle.

Motomura is directed to a parallel processor system which executes a plurality of threads in parallel with the help of an "ordered multithread executing system." (Motomura, col. 8, ll. 1-12). A processor is capable of forking threads during execution by transmitting a fork demand to the ordered multithread executing system, as well as by sending a thread descriptor. (Motomura, col. 8, ll. 13-23). When a processor "initiates execution of a new thread, the processor request[s] the thread descriptor of the new executable thread from the ordered multithread executing system via the demand transfer line." (Motomura, col. 8, ll. 27-31). The processor will subsequently generally receive the information necessary to begin processing the thread. (Motomura, col. 8, ll. 31-39).

Appellants' claim 1 and Motomura are very different. Appellants' claim 1 recites executing "instructions from more than one of the plurality of threads concurrently in a clock cycle." In Motomura, each processor can execute only one thread at a time, as it is disclosed that each thread must go into a "waiting" or "completed" state before another thread is assigned to the processor. (Motomura, col. 8, ll. 40-51). In contrast, Appellants' specification supports the claim language by disclosing that "[e]ach of the [processing slices] operates by interleaving the execution of instructions from the four threads, including the ability to execute several instructions concurrently in the same clock cycle." (Specification, p. 8, ll. 23-25).

The Examiner subsequently states that the ability to execute instructions concurrently in the same clock cycle is supported by Motomura's ability to fork threads

such that other threads are simultaneously performing an execution, decode, or fetch step. (Office Action, p. 2). However, since each processor (Motomura, FIG. 1, element 110) in Motomura can only execute one thread at a time, it is necessary to consider the entire parallel processor system (Motomura, FIG. 1, element 100) as the processing slice, as the Examiner concedes. (Office Action, p. 2).

Accordingly, it cannot be the case that the ordered multithread executing system is analogous to the "peripheral unit" of independent claim 1. If the parallel processor system of Motomura is equivalent to a processing slice in Appellants' claim 1, then there is no analogous "peripheral unit" disclosed in Motomura, as the alleged "peripheral unit" (the ordered multithread executing system) would therefore be contained within the processing slice of claim 1.

Assuming, *arguendo*, that the sum total of processors disclosed in Motomura are analogous to a single processing slice as in claim 1, the Examiner's rejection nonetheless fails for want of a "functional unit", which under the Examiner's present scenario is analogous to a single processor in Motomura. Accordingly, the Examiner's mapping of elements from Motomura is inconsistent, and cannot support the purported analogy.

Since Motomura does not teach or suggest each and every feature of independent claim 1 it does not anticipate that claim. Accordingly, the Examiner's rejection of claim 1 must be reversed. Furthermore, dependent claims 2-7 and 10-12 are also not anticipated by Motomura for at least the same reasons as independent claim 1 from which they depend and further in view of their own respective features. Accordingly, the Examiner's rejection of claims 2-7 and 10-12 must also be reversed.

2. The Anticipation Rejection with Respect to Claims 14-20 and 23-25 is in Error and Must be Reversed

Appellants' independent claim 14 recites a method for which the apparatus of claim 1 is a physical embodiment as discussed above. Claim 14 is distinguishable over Motomura for at least the same reasons as claim 1. Since Motomura does not teach or suggest each and every feature of independent claim 14 it does not anticipate that claim. Accordingly, the Examiner's rejection of claim 14 must be reversed. Furthermore, dependent claims 15-21, 24, and 25 are also not anticipated by Motomura for at least the same reasons as independent claim 14 from which they depend and further in view of their own respective features. Accordingly, the Examiner's rejection of claims 15-20 and 23-25 must also be reversed.

3. The Anticipation Rejection with Respect to Claims 27-33 and 36-38 is in Error and Must be Reversed

Appellants' independent claim 27 recites a processing system comprising similar features as independent claim 1 discussed above. Claim 27 is distinguishable over Motomura for at least the same reasons as claim 1. Since Motomura does not teach or suggest each and every feature of independent claim 27 it does not anticipate that claim. Accordingly, the Examiner's rejection of claim 27 must be reversed. Furthermore, dependent claims 28-33 and 36-38 are also not anticipated by Motomura for at least the same reasons as independent claim 1 from which they depend and further in view of their own respective features. Accordingly, the Examiner's rejection of claims 28-33 and 36-38 must also be reversed.

4. The Anticipation Rejection with Respect to Claim 41 is in Error and Must be Reversed

Appellants' independent claim 41 recites a processing system comprising similar features as independent claim 1 discussed above. Claim 41 is distinguishable over Motomura for at least the same reasons as claim 1. Since Motomura does not teach or

suggest each and every feature of independent claim 41 it does not anticipate that claim. Accordingly, the Examiner's rejection of claim 41 must be reversed.

5. The Anticipation Rejection with Respect to Claims 8 and 9 is in Error and Must be Reversed

Claims 8 and 9 are dependent on claim 1, and are distinguishable over Motomura for at least the same reasons as independent claim 1. Since Motomura does not teach or suggest each and every feature of independent claim 1, is does not anticipate claims 8 and 9. Assuming, *arguendo*, that Motomura does teach or suggest each and every feature of independent claim 1, dependent claims 8 and 9 are further distinguishable over Motomura for the following reasons.

Appellants' claim 8 recites the apparatus of claim 1 "wherein the processing slice disables the first thread after sending the command message if the command message is a wait instruction." In contrast, claim 9 recites the apparatus of claim 1 "wherein the first thread continues to execute after sending the command message if the command message is a non-wait instruction."

The Examiner has rejected claims 8 and 9 over Motomura, stating that "Motomura discloses executing a different thread while the first thread is in a waiting state (column 8, lines 40-42). Motomura's switching to different thread is the claimed disabling the first thread. Motomura discloses an executing scenario which executing a program sequentially without dividing. [sic] The disclosed executing a program without dividing is the claimed continuing to execute if a non-wait instruction." (Office Action, p. 4)

However, Motomura discloses that a possible reason for a thread to enter the waiting state, "is to read data in the memory in another processor or because of a failure of synchronizing operations." (Motomura, col. 1, ll. 36-39).

Note that the "command message" identified in claims 8 and 9 refers to the command message of claim 1 which is used to specify a peripheral operation. A peripheral operation in Motomura, assuming that the analogous peripheral is the ordered multithread executing system, does not cause threads in the Motomura system to be disabled or switched. Furthermore, operations transmitted to the ordered multithread executing system do not come in "wait" and "non-wait" variants. Accordingly, it cannot be the case that the ordered multithread executing system is the peripheral unit to which command messages are sent, while those command messages simultaneously cause a thread to be disabled by a processing slice.

Since Motomura does not teach or suggest each and every feature of claims 8 and 9 it does not anticipate those claims. Accordingly, the Examiner's rejection of claims 8 and 9 must be reversed.

6. The Anticipation Rejection with Respect to Claims 21 and 22 is in Error and Must be Reversed

Claims 21 and 22 are dependent on claim 14, and are distinguishable over Motomura for at least the same reasons as independent claim 14. Since Motomura does not teach or suggest each and every feature of independent claim 14, is does not anticipate claims 21 and 22. Assuming, *arguendo*, that Motomura does teach or suggest each and every feature of independent claim 14, dependent claims 21 and 22 are further distinguishable over Motomura for similar reasons to claims 8 and 9, above.

Since Motomura does not teach or suggest each and every feature of claims 21 and 22 it does not anticipate those claims. Accordingly, the Examiner's rejection of claims 21 and 22 must be reversed.

7. The Anticipation Rejection with Respect to Claims 34 and 35 is in Error and Must be Reversed

Claims 34 and 35 are dependent on claim 27, and are distinguishable over Motomura for at least the same reasons as independent claim 27. Since Motomura does not teach or suggest each and every feature of independent claim 27, is does not anticipate claims 34 and 35. Assuming, *arguendo*, that Motomura does teach or suggest each and every feature of independent claim 27, dependent claims 34 and 35 are further distinguishable over Motomura for similar reasons to claims 8 and 9, above.

Since Motomura does not teach or suggest each and every feature of claims 34 and 35 it does not anticipate those claims. Accordingly, the Examiner's rejection of claims 34 and 35 must be reversed.

B. Rejection of claims 13, 26, and 39 under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 5,815,727 to Motomura in view of U.S. Patent No. 5,418,917 to Hiraoka et al.

The Final Office Action mailed on July 19, 2005 rejected claims 13, 26, and 39 under 35 U.S.C. § 103(a) as allegedly being obvious over Motomura in view of Hiraoka.

1. The Obviousness Rejection with Respect to Claim 13 is in Error and Must be Reversed

Claim 13 depends from independent claim 1 and includes the features recited therein. Hiraoka does not overcome the deficiencies of Motomura relative to claim 1, described above. For this reason, the rejection of claim 13 must be reversed.

2. The Obviousness Rejection with Respect to Claim 26 is in Error and Must be Reversed

Claim 26 depends from independent claim 14 and includes the features recited therein. Hiraoka does not overcome the deficiencies of Motomura relative to claim 14, described above. For this reason, the rejection of claim 26 must be reversed.

3. The Obviousness Rejection with Respect to Claim 39 is in Error and Must be Reversed

Claim 39 depends from independent claim 27 and includes the features recited therein. Hiraoka does not overcome the deficiencies of Motomura relative to claim 27, described above. For this reason, the rejection of claim 39 must be reversed.

C. Rejection of claim 40 under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 5,815,727 to Motomura in view of U.S. Patent No. 5,938,765 to Dove et al.

The Final Office Action mailed on July 19, 2005 rejected claim 40 under 35 U.S.C. § 103(a) as allegedly being obvious over Motomura in view of Dove.

1. The Obviousness Rejection with Respect to Claim 40 is in Error and Must be Reversed

Claim 40 discloses a similar set of features as disclosed in independent claim 1, but further discloses a "plurality of multi-thread processors" and a "plurality of peripheral units." The Examiner concedes that Motomura does not teach a "plurality of multi-thread processors" and relies on Dove to supply the missing teaching. However, neither Motomura or Dove teaches the missing features discussed above with regard to independent claim 1, such as a processing slice "capable of executing the instructions from more than one of the plurality of threads concurrently in a clock cycle." The rejection of claim 40 further suffers from the same impossible analogy to Motomura as claim 1, and Dove does not remedy the deficiency.

Furthermore, neither Motomura nor Dove teach or suggest a "plurality of peripheral units" as required by independent claim 40. Accepting, *arguendo*, the

Examiner's characterization of Motomura, the ordered multithread executing system is the single peripheral unit in the Motomura system (as discussed above with reference to independent claim 1, it is furthermore the case that the ordered multithread executing system cannot be properly characterized as a peripheral unit). The Examiner does not indicate where the missing teaching of a "plurality of peripheral units" may be found in either reference, such as may be coupled over a peripheral bus to transfer peripheral information.

Since the combination of Motomura and Dove does not teach or suggest each and every feature of independent claim 40, it cannot render obvious that claim. Accordingly, the rejection of claim 40 must be reversed.

D. Conclusion

The subject matter of claims 1-41 is patentable over the cited prior art because the Examiner has failed to make a *prima facie* case of anticipation or obviousness. Therefore, Appellants respectfully request that the Board reverse the Examiner's final rejection of these claims under 35 U.S.C. § 102 and 35 U.S.C. § 103 and remand this application for issue.

Respectfully submitted,

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VIII. Claims Appendix

1. An apparatus comprising:

a peripheral bus coupled to a peripheral unit to transfer peripheral information including a command message specifying a peripheral operation; and

a processing slice coupled to the peripheral bus to execute a plurality of threads comprising instructions, the plurality of threads including a first thread sending the command message to the peripheral unit;

wherein the processing slice comprises a functional unit to perform a register operation specified in the instructions dispatched from each of the plurality of threads; and

wherein the processing slice executes the instructions from more than one of the plurality of threads concurrently in a clock cycle.

2. The apparatus of claim 1 wherein the peripheral unit is one of an input device and an output device.

3. The apparatus of claim 1 wherein the peripheral operation is one of an input operation and an output operation.

4. The apparatus of claim 1 wherein the command message includes at least one of a message content, a peripheral address identifying the peripheral unit, and a command code specifying the peripheral operation.

5. The apparatus of claim 1 wherein the peripheral information includes a response message sent from the peripheral unit to the processing slice, the response message indicating the peripheral operation is completed.

6. The apparatus of claim 5 wherein the response message includes at least one of a thread identifier identifying the first thread, an operation result of the peripheral operation, a data register address specifying a data register in the processing slice to store the operation result, and a length indicator indicating length of the response message.

7. The apparatus of claim 6 wherein the peripheral bus comprises:

a bi-directional bus to transfer the command message from the processing slice to the peripheral unit and the response message from peripheral unit to the processing slice.

8. The apparatus of claim 1 wherein the processing slice disables the first thread after sending the command message if the command message is a wait instruction.

9. The apparatus of claim 1 wherein the first thread continues to execute after sending the command message if the command message is a non-wait instruction.

10. The apparatus of claim 8 wherein the processing slice enables the first thread after receiving the response message from the peripheral unit if the first thread was disabled.

11. The apparatus of claim 1 wherein the processing slice comprises:

an instruction processing unit to process instructions fetched from a program memory; and

a thread control unit coupled to the instruction processing unit to manage initiating and termination of at least one of the plurality of threads.

12. The apparatus of claim 11 wherein the processing slice further comprises:

a memory access unit coupled to the instruction processing unit to provide access to one of a plurality of data memories via a data memory switch, the memory access unit having a plurality of data base registers, each of the data base registers corresponding to each of the threads; and

a register file coupled to the instruction processing unit and a peripheral message unit having a plurality of data registers, each of the data registers corresponding to each of the threads.

13. The apparatus of claim 12 wherein the instruction processing unit comprises:

an instruction fetch unit to fetch the instructions from the program memory using a plurality of program counters, each program counter corresponding to each of the threads;

an instruction buffer coupled to the instruction fetch unit to hold the fetched instructions; and

an instruction decoder and dispatcher coupled to the instruction buffer to decode the instructions and dispatch the decoded instructions to one of the memory access unit, the functional unit, and the peripheral unit.

14. A method comprising:

transferring peripheral information to a peripheral unit via a peripheral bus, the peripheral information including a command message specifying a peripheral operation; and

executing a plurality of threads comprising instructions by a processing slice, the plurality of threads including a first thread sending the command message to the peripheral unit;

wherein the processing slice comprises a functional unit to perform a register operation specified in the instructions dispatched from each of the plurality of threads; and

wherein the processing slice executes the instructions from more than one of the plurality of threads concurrently in a clock cycle.

15. The method of claim 14 wherein the peripheral unit is one of an input device and an output device.

16. The method of claim 14 wherein the peripheral operation is one of an input operation and an output operation.

17. The method of claim 14 wherein the command message includes at least one of a message content, a peripheral address identifying the peripheral unit, and a command code specifying the peripheral operation.

18. The method of claim 14 wherein the peripheral information includes a response message sent from the peripheral unit to the processing slice, the response message indicating the peripheral operation is completed.

19. The method of claim 18 wherein the response message includes at least one of a thread identifier identifying the first thread, an operation result of the peripheral operation, a data register address specifying a data register in the processing slice to store the operation result, and a length indicator indicating length of the response message.

20. The method of claim 19 wherein transferring the peripheral information comprises:

transferring the command message from the processing slice to the peripheral unit and the response message from peripheral unit to the processing slice via a bi-directional bus.

21. The method of claim 14 wherein executing the plurality of threads comprises disabling the first thread after sending the command message if the command message is a wait instruction.

22. The method of claim 14 wherein executing the plurality of threads comprises continuing executing the first thread after sending the command message if the command message is a non-wait instruction.

23. The method of claim 21 wherein executing the plurality of threads comprises enabling the first thread after receiving the response message from the peripheral unit if the first thread was disabled.

24. The method of claim 14 wherein executing the plurality of threads comprises:

processing instructions fetched from a program memory by an instruction processing unit;

managing initiating and termination of at least one of the plurality of threads by a thread control unit.

25. The method of claim 24 wherein executing the plurality of threads further comprises:

accessing to one of a plurality of data memories by a memory access unit via a data memory switch, the memory access unit having a plurality of data base registers, each of the data base registers corresponding to each of the threads; and

storing data in a register file having a plurality of data registers, each of the data registers corresponding to each of the threads.

26. The method of claim 25 wherein processing instructions comprises:

fetching the instructions from the program memory using a plurality of program counters by an instruction fetch unit, each program counter corresponding to each of the threads;

holding the fetched instructions in an instruction buffer; and

decoding the instructions and dispatching the decoded instructions by an instruction decoder and dispatcher to one of the memory access unit, the functional unit, and the peripheral unit.

27. A processing system comprising:

a plurality of banks of data memory;

a data memory switch coupled to the banks of data memory;

a program memory to store a program;

a peripheral bus coupled to a peripheral unit to transfer peripheral information including a command message specifying a peripheral operation; and

a processing slice coupled to the peripheral bus to execute a plurality of threads comprising instructions, the plurality of threads including a first thread sending the command message to the peripheral unit;

wherein the processing slice comprises a functional unit to perform a register operation specified in the instructions dispatched from each of the plurality of threads; and

wherein the processing slice executes the instructions from more than one of the plurality of threads concurrently in a clock cycle.

28. The processing system of claim 27 wherein the peripheral unit is one of an input device and an output device.

29. The processing system of claim 27 wherein the peripheral operation is one of an input operation and an output operation.

30. The processing system of claim 27 wherein the command message includes at least one of a message content, a peripheral address identifying the peripheral unit, and a command code specifying the peripheral operation.

31. The processing system of claim 27 wherein the peripheral information includes a response message sent from the peripheral unit to the processing slice, the response message indicating the peripheral operation is completed.

32. The processing system of claim 31 wherein the response message includes at least one of a thread identifier identifying the first thread, an operation result of the peripheral operation, a data register address specifying a data register in the

processing slice to store the operation result, and a length indicator indicating length of the response message.

33. The processing system of claim 32 wherein the peripheral bus comprises:

a bi-directional bus to transfer the command message from the processing slice to the peripheral unit and the response message from peripheral unit to the processing slice.

34. The processing system of claim 27 wherein the processing slice disables the first thread after sending the command message if the command message is a wait instruction.

35. The processing system of claim 27 wherein the first thread continues to execute after sending the command message if the command message is a non-wait instruction.

36. The processing system of claim 34 wherein the processing slice enables the first thread after receiving the response message from the peripheral unit if the first thread was disabled.

37. The processing system of claim 27 wherein the processing slice comprises: an instruction processing unit to process instructions fetched from a program memory; and

a thread control unit coupled to the instruction processing unit to manage initiating and termination of at least one of the plurality of threads.

38. The processing system of claim 37 wherein the processing slice further comprises:

a memory access unit coupled to the instruction processing unit to provide access to one of the plurality of data memories via the data memory switch, the memory access unit having a plurality of database registers, each of the data base registers corresponding to each of the threads; and

a register file coupled to the instruction processing unit and a peripheral message unit having a plurality of data registers, each of the data registers corresponding to each of the threads.

39. The processing system of claim 38 wherein the instruction processing unit comprises:

an instruction fetch unit to; fetch the instructions from the program memory using a plurality of program counters; each program counter corresponding to each of the threads;

an instruction buffer coupled to the instruction fetch unit to hold the fetched instructions; and

an instruction decoder and dispatcher coupled to the instruction buffer to decode the instructions and dispatch the decoded instructions to one of the memory access unit, the functional unit, and the peripheral unit.

40. A processing system comprising:

a plurality of multi-thread processors;

a plurality of peripheral units;

a peripheral bus coupled to the peripheral units to transfer peripheral information between the multi-thread processors and the peripheral units, the peripheral information including a command message sent from one of the multi-thread processors to one of the peripheral units;

wherein each processor comprises a plurality of processing slices to execute a plurality of threads comprising instructions including the command message;

wherein each processing slice comprises a functional unit to perform a register operation specified in the instructions dispatched from each of the plurality of threads; and

wherein the processing slice is capable of executing the instructions from more than one of the plurality of threads concurrently in a clock cycle.

41. A processing system comprising:

a multi-thread processor having program base registers and data base registers;

at least one peripheral unit;

a peripheral bus coupled to the at least one peripheral unit to transfer peripheral information between the multi-thread processor and the at least one peripheral unit, the peripheral information including a command message sent from the multi-thread processor to the peripheral unit;

wherein the processor comprises a plurality of processing slices to execute a plurality of threads comprising instructions including the command message;

wherein each processing slice comprises a functional unit to perform a register operation specified in the instructions dispatched from each of the plurality of threads; and

wherein the processing slice is capable of executing the instructions from more than one of the plurality f threads concurrently in a clock cycle.

IX. Evidence Appendix

To the best of the knowledge of Appellants, Appellants' legal representative, and Appellants' assignee, there has been no evidence submitted pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132, nor has any other evidence been entered in the record by the Examiner and relied upon in this Appeal Brief.

X. Related Proceedings Appendix

To the best of the knowledge of Appellants, Appellants' legal representative, and Appellants' assignee, there are no other appeals or interferences which will directly affect or be directly affected or have a bearing on a decision by the Board of Patent Appeals and Interferences ("the Board") in the pending appeal.

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